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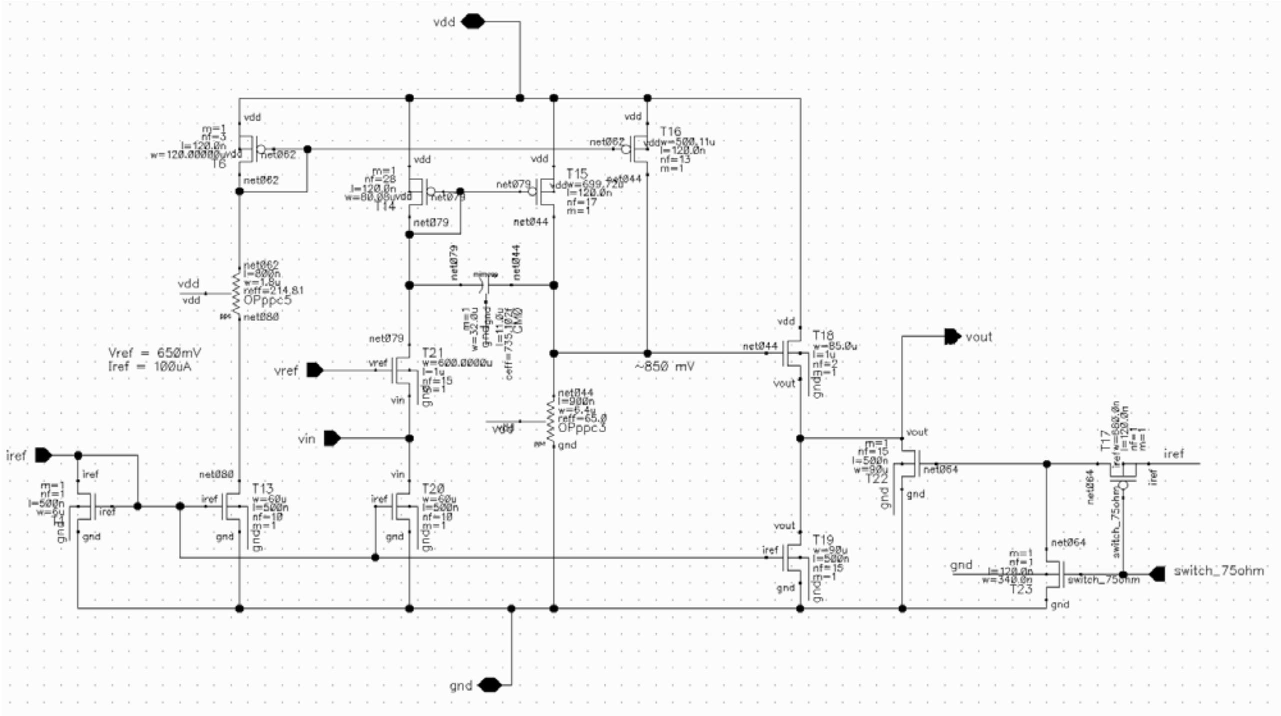
EECS 413 Miniproject: A Switched-Impedance Video Repeater

1. Circuit Topology

The design specifications are realized here by a two-stage amplifier, shown below. The input common-gate stage maintains the required input impedance and provides the required gain component. Rather than using a traditional common-gate stage, however, the load resistor is buffered via a current-mirror, significantly decreasing the circuit's sensitivity to VDD while also allowing the output impedance to be changed independently of the gain (discussed in Section 2).



The output common-drain stage provides the required output impedance. A switchable current source is used to change the stage’s bias current, and thus its impedance. Finally, a current source on its gate provides the relatively high quiescent voltages needed to operate the stage in strong saturation.

2. Analysis

2.1 Biasing

In order to ensure accurate transfer from theory to simulation, strict design rules must be met. Here, because of tight headroom requirements, we choose $V_{DS} > V_{GS} - V_{TH} + 100\text{mV}$ and $V_{GS} > V_{TH} + 100\text{mV}$.

The input stage is biased, via the NMOS current mirror, at 1.08mA, chosen so all transistors are able to remain in strong saturation, as previously defined.

Since the load resistor must be so small, it doesn’t provide a large enough quiescent voltage to properly bias the output stage on its own, so a current source is used to drive the load resistor with a DC bias current, increasing the quiescent voltage without affecting AC performance.

2.2 Input impedance

To achieve an input impedance of 50 ohms, we take $Z_{in} \approx \frac{1}{(g_m + g_{mb})}$. Assuming $g_{mb} \approx 0.1 g_m$, we find gm = 0.018. Achieving this is simply a matter of sizing the gain transistor such that $\frac{W}{L} = \frac{{g_m}^2}{2\mu_n C_{ox} I_D}$. The absolute size (W and L individually) determines V_{GS} and can be found by solving the transistor's current-law equation.

2.3 Output Impedance

The output impedance is approached similar to the input impedance, with two differences. First, the impedance of the circuit is varied by changing the bias current. To do so, two bias transistors act in parallel with one transistor attached to an analog switch. The switch is controlled by the switch_75ohm input, and turns the second transistor on when switch_75ohm is low and off when it is high. By noting this circuit's similarity to a digital inverter, it is easy to justify using digital-style sizing techniques (i.e. NMOS sized to minimum length and the PMOS sized to twice that of the NMOS).

Secondly, the large bandwidth requirement means that the approximation $Z_{out} = \frac{1}{(g_m + g_{mb})}$ is not accurate overall. While at low frequencies it reasonable, the actual output impedance quickly drifts towards the output impedance of the previous stage as the frequency increases. Therefore, in order to maintain stable impedance over frequency, the output impedance of the previous stage must also be controlled. Since the difference between the two desired output impedances is not large (25 ohms), it is sufficient to choose the output impedance for the first stage somewhere between the two. Here, 65 ohms has been used.

2.4 Gain

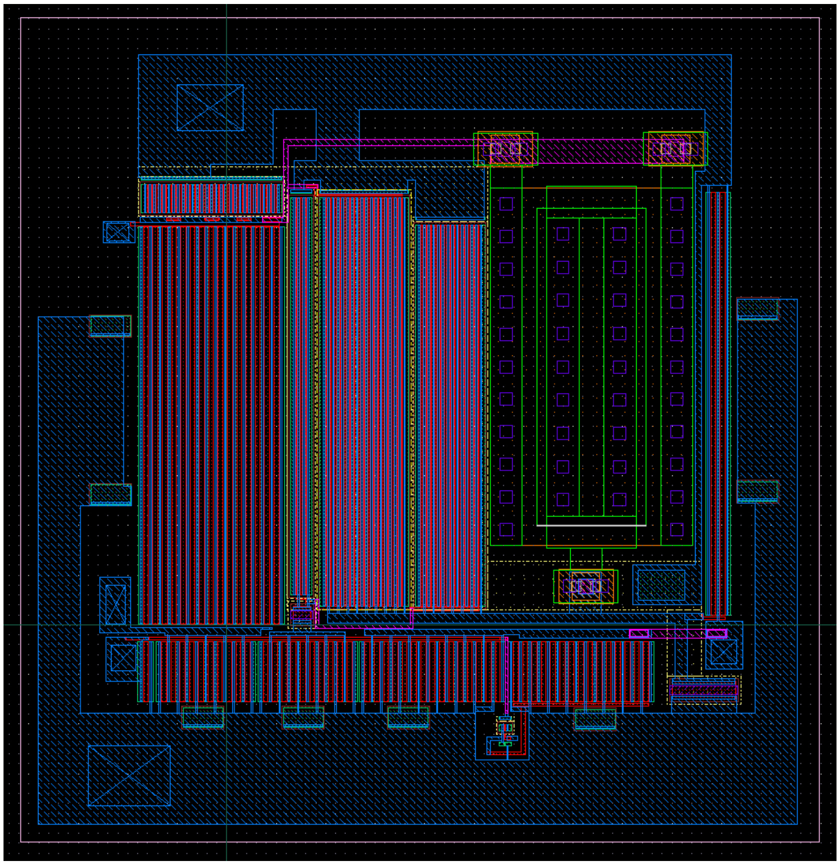
A traditional common-gate stage has a gain, $A_v = g_m R_D$. However, because we need a small output impedance of around 65 ohms (see section 2.3), it is necessary to use a smaller load resistor than is practical. Since current gain in the current mirror is approximately equal to the ratio of the sizes, it can be said that the mirror multiplies the g_m seen on the load side by this ratio. By requiring a gain of 7 (accounting for non-idealities in the output stage) and R_L = 65, we see the current gain of the impedance transformer needs to be $\frac{W/L_1}{W/L_2} \approx 6$.

Unfortunately, an impedance mismatch develops between the two stages at high frequencies. The input impedance of the output stage looks like $Z_{in\_CD} = \frac{1}{sC_{GS}}(1+\frac{g_m}{g_{mb}}) + \frac{1}{g_{mb}} \xrightarrow{s=\infty} \frac{1}{g_{mb}}$. Thus, in 50 ohm mode, the loss due to this mismatch is $\frac{1}{1+65g_{mb}} \approx 0.89$, whereas in 75 ohm mode, this loss becomes ≈ 0.92. The change seen is actually somewhat larger in practice, likely due to an inaccurate estimation of g_{mb} used here.

3. Layout

The layout presented its own challenges. Upon first PEX extraction, the bandwidth dropped to under

100MHz. However, by iteratively locating any large resistances in the resulting netlist and adjusting wire sizes and routing to minimize these resistances (paying special attention to signal-carrying traces), I was able to achieve results very similar to my original simulations.



4. Simulation

The circuit was simulated over Process, Supply Voltage, and Temperature variations (PVT). Below are the results, followed by a table summarizing the important performance characteristics they show. Of note is the fact that the output impedance (both settings) and bandwidth maintains +/- 10% of spec. over PVT. The input impedance maintains +20 / -5% error over PVT, but is slightly low at nominal conditions. I suspect these absolute errors are due to incorrectly-sized transistors (as a result of troubleshooting early on that had accidentally propagated through the design/simulation process). Specifically, T21 should have W = 300u, not 600u.

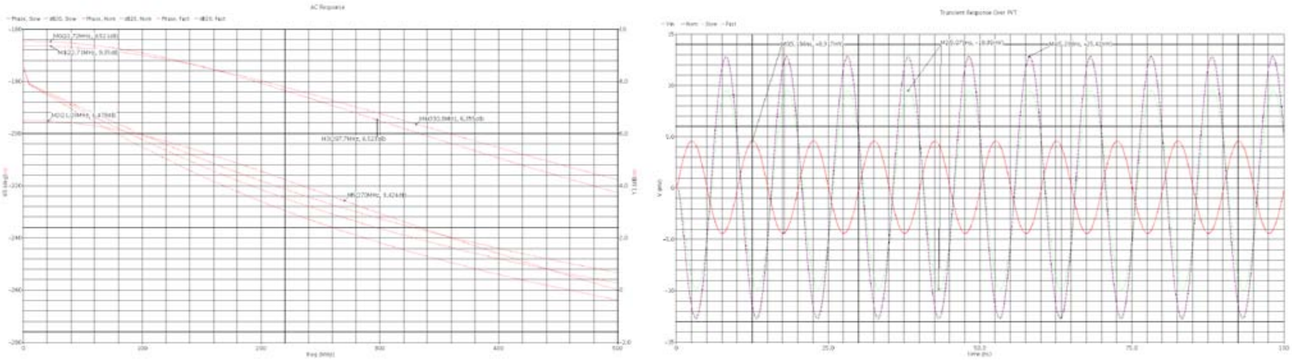


Figure 1: (left) Frequency Response over PVT, (right) Transient Response due to a 10mV input signal.

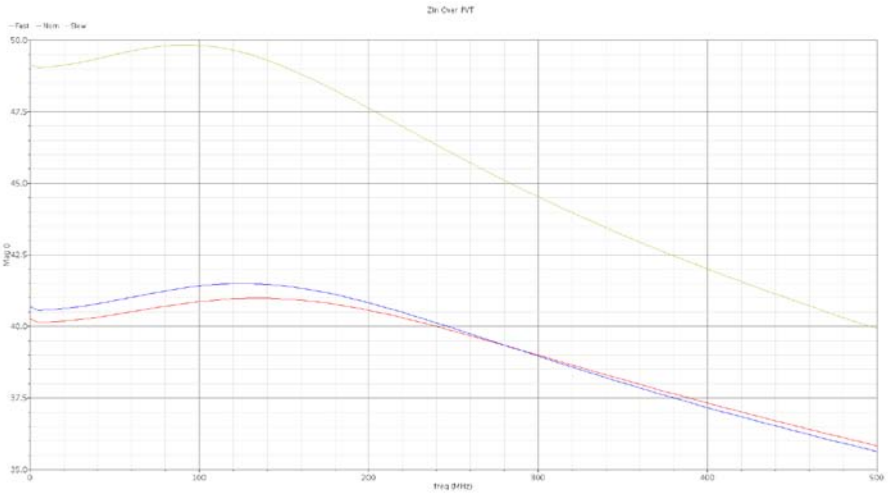


Figure 2: Input Impedance over PVT

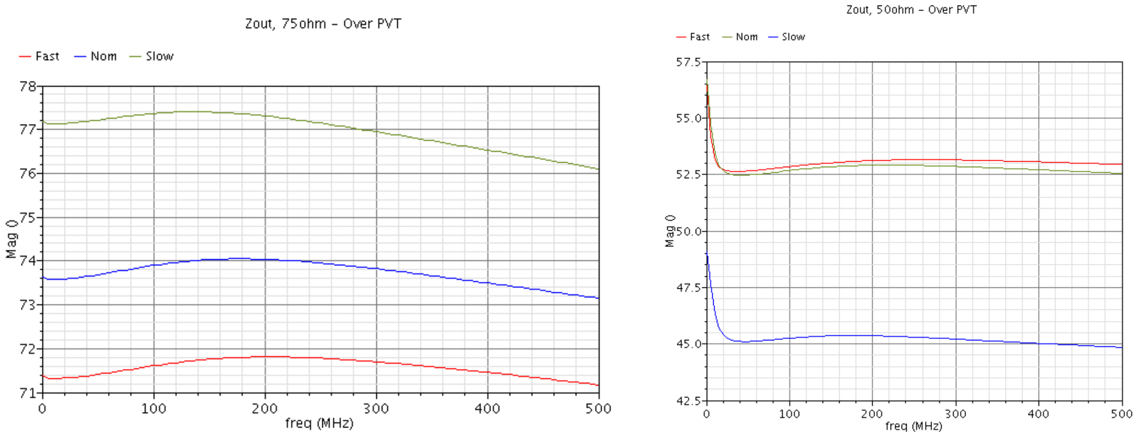


Figure 3: Output Impedance over PVT for (left) 75 ohm Case, (right) 50 ohm Case

5. Performance Summary

	Slow PVT Corner	**Nominal PVT Corner**	**Fast PVT Corner**
Low Frequency Gain	6.478 dB	9.521 dB	9.35 dB
-3dB Frequency (MHz)	270	297.7	330.8
Input Impedance (ohms) Min:	45	38.2	38.2
Max:	50	41.2	40.8
Output Impedance, 50ohm Min:	48.2	52.5	52.5
50ohm Max:	45	57	57
75ohm Min:	77.1	73.5	71.2
75ohm Max:	77.5	74	71.8